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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,116	03/31/2004	Shun-ichi Miyazaki	042164	3705

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EXAMINER	
LE, THI Q	

ART UNIT	PAPER NUMBER
2613	

MAIL DATE	DELIVERY MODE
06/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/813,116	MIYAZAKI ET AL.	
	Examiner	Art Unit	
	Thi Q. Le	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Action is in response to Applicant's amendment filed on 3/27/2007. **Claims 4-13** are still pending in the present application.

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Information Disclosure Statement

2. The information disclosure statements (IDS) filed on 3/31/2004, 6/01/2005, 8/17/2005 were considered by the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 4, 6, 7, 9 and 12** are rejected under 35 U.S.C. 102(b) as being anticipated by **Nagata (US Patent # 3,659,159)**.

Consider **claim 4**, Nagata clearly shows and discloses, an optical signal processing apparatus comprising: at least one photodiode (read as, photoelectric conversion element 42 (note, the operation of the circuit of figure 4 is the same as that of figure 3; thus the photoelectric

conversion element 42 can also be a photodiode, column 3 lines 67-70); figure 4) for converting an optical signal to an electrical signal; a resistor (read as, resistor 49; figure 4) having its one end connected to an anode of this photodiode (note, the resistor 49 is connected to the photodiode 42 when the switch is closed); and a resonant tunneling diode (read as, tunneling diode 43; figure 4) having one end connected to the one end of this resistor (note, the resistor 49 is also connected to tunneling diode 43, when the switch is closed; figure 4); wherein a digital signal is acquired by switch operation of the resonant tunneling diode (column 2 lines 65-75) (figure 4; column 3 lines 51-67; column 2 lines 65-75).

Consider **claim 6, and as applied to claim 4 above**, Nagata further discloses, wherein an electrical signal is acquired by the switch operation of the resonant tunneling diode (figure 3; column 2 line 65- column 3 line 16).

Consider **claim 7**, Nagata clearly shows and discloses, an optical signal processing apparatus comprising: at least one photodiode (read as, photoelectric conversion element 42; figure 4) for converting an optical signal to an electrical signal; a first resistor (read as, resistor 49; figure 4) having its one end connected to an anode of this photodiode note, the resistor 49 is connected to the photodiode 42 when the switch is closed); a resonant tunneling diode (read as, tunneling diode 43; figure 4) having its one end connected to the one end of this resistor (note, the resistor 49 is also connected to tunneling diode 43, when the switch is closed; figure 4); and a second resistor (read as, resistor 47; figure 4) having its one end connected to the other end of the resonant tunneling diode; wherein a digital signal is acquired by switch operation of the resonant tunneling diode (column 2 lines 65-75) (figure 4; column 3 lines 51-67; column 2 lines 65-75).

Consider **claim 9, and as applied to claim 7 above**, claim 9 is rejected for the same reason as claim 6 above.

Consider **claim 12, and as applied to claims 4 and 6 above**, Nagata further discloses, wherein at least the photodiode (read as, photo-conductive element PE; figure 9j) and the resonant tunneling diode (read as, tunneling diode TD; figure 9j) are formed on the same semiconductor substrate (figure 9j; column 5 lines 30-71).

Consider **claim 12, and as applied to claims 7 and 9 above**, claim 12 is rejected for the same reason as claim 12 applied to claims 4 and 6, above.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. **Claims 5, 8, 12 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Nagata (US Patent # 3,659,159)** in view of **Moise et al. (US Patent # 6,008,917)**.

Consider **claim 5, and as applied to claim 4 above**, Nagata disclosed a light emitter 32, as shown in figure 3, and the invention as described above; Nagata differs from the present invention in that it does not disclose an optical modulator connected to the one end of the resonant tunneling diode, changing its transmittance, and modulating and outputting light.

In related art, Moise et al. disclose an optical modulator (read as, lasing device 16; figure 1) connected to the one end of the resonant tunneling diode, changing its transmittance, and modulating and outputting light (note, the lasing device generates and modulates an output light in response to the first and second voltage levels from the tunneling diode) (figure 1; abstract; column 2 lines 1-5).

It would have been obvious for a person of ordinary skill in the art at the time of the invention to incorporate the teachings of Moise et al. with Nagata. Because, having a constant output of light while modulating the constant light source using an integrated or externally modulator provides higher transmission bit-rate.

Consider **claim 12, and as applied to claim 5 above**, claim 12 is rejected for the same reason as claim 12 applied to claims 4 and 6, above.

Consider **claim 13, and as applied to claims 5 above**, Nagata as modified by Moise et al. further disclose, wherein at least the photodiode (read as, photo-conductive element PE; Nagata, figure 9j), the resonant tunneling diode (read as, tunneling diode TD; Nagata, figure 9j) and the optical modulator (read as, laser diode LD; Nagata, figure 9j) are formed on the same semiconductor substrate (Nagata, figure 9j; column 5 lines 30-71).

Consider **claim 8 and as applied to claim 7 above**, claim 8 is rejected for the same reason as claim 5 above.

Consider **claim 12, and as applied to claim 8 above**, claim 12 is rejected for the same reason as claim 12 applied to claims 4 and 6, above.

Consider **claim 13, and as applied to claim 8 above**, claim 13 is rejected for the same reason as claim 13 applied to claim 5, above.

9. **Claims 10** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Nagata (US Patent # 3,659,159)** in view of **Cornely et al. (US Patent # 3,319,080)**.

Consider **claim 10, and as applied to claims 4, 6, 7, 9 above**, Nagata disclosed the invention as described above, except for, wherein the photodiodes are provided at least in parallel.

In related art, Cornely et al. disclose, wherein the photodiodes (read as, photodiodes 18; figure 1) are provided at least in parallel (figure 1, column 2 lines 30-41).

It would have been obvious for a person of ordinary skill in the art at the time of the invention to incorporate the teachings of Cornely et al. with Nagata. Because, using a plurality of photodiode allow for receiving a plurality of signal for processing.

10. **Claim 11** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Nagata (US Patent # 3,659,159)** in view of **Amano et al. (US Patent # 5,451,767).**

Consider **claim 11, and as applied to claims 4, 6, 7, 9 above**, Nagata disclosed the invention as described above, except for, wherein the photodiodes are provided at least in series.

In related art Amano disclose an optical modulator gate array. Wherein the photodiodes are provided at least in series (read as, the photodiodes PD1-PDn are connected in series with each other to form a logical NAND gate operation; figure 32a, column 28 lines 52-67).

It would have been obvious for a person of ordinary skill in the art at the time of the invention to incorporate the teachings of Amano with Nagata. Since the structural formation of the array of photodiodes allows for logical operation (i.e. NAND, OR, AND, etc) of the optical modulator.

11. **Claim 10** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Nagata (US Patent # 3,659,159)** in view of **Moise et al. (US Patent # 6,008,917)** and further in view of **Cornely et al. (US Patent # 3,319,080).**

Consider **claim 10, and as applied to claim 5 above**, Nagata as modified by Cornely et al. disclosed the invention as described above, except for, wherein the photodiodes are provided at least in parallel.

In related art, Cornely et al. disclose, wherein the photodiodes (read as, photodiodes 18; figure 1) are provided at least in parallel (figure 1, column 2 lines 30-41).

It would have been obvious for a person of ordinary skill in the art at the time of the invention to incorporate the teachings of Cornely et al. with Nagata as modified by Cornely et al. Because, using a plurality of photodiode allow for receiving a plurality of signal for processing.

Consider **claim 10, and as applied to claim 8 above**, claim 10 is rejected for the same reason as claim 10 applied to claim 2, above.

12. **Claim 11** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Nagata (US Patent # 3,659,159)** in view of **Moise et al. (US Patent # 6,008,917)** and further in view of **Amano et al. (US Patent # 5,451,767).**

Consider **claim 11, and as applied to claims 5 above**, Nagata disclosed the invention as described above, except for, wherein the photodiodes are provided at least in series.

In related art Amano disclose an optical modulator gate array. Wherein the photodiodes are provided at least in series (read as, the photodiodes PD1-PDn are connected in series with each other to form a logical NAND gate operation; figure 32a, column 28 lines 52-67).

It would have been obvious for a person of ordinary skill in the art at the time of the invention to incorporate the teachings of Amano with Nagata. Since the structural formation of the array of photodiodes allows for logical operation (i.e. NAND, OR, AND, etc) of the optical modulator.

Consider **claim 11, and as applied to claim 8 above**, claim 11 is rejected for the same reason as claim 11 applied to claim 5, above.

Response to Arguments

13. Applicant's arguments, filed 3/27/2007, see pages 6-7, with respect to the rejection(s) of claim(s) 4, 7 have been fully considered but they are not persuasive.

On page 6, the applicant argues, the optoelectronic amplifier circuit, as shown in Fig. 4, of Nagata, see col.4, lines 63-64, does not include at least one photodiode for converting an optical signal to an electrical signal, as called for in claim 4, since instead the optoelectronic amplifier of Fig. 4 includes either a photo-transistor or a solar battery, but not a photodiode, as the photoelectric conversion element 42. The Examiner respectfully disagrees, since Nagata clearly stated in column 3 lines 67-70, the circuit of figure 4 operates the same way as that of the circuit of figure 3. Further, the operation of the photoelectric conversion element 42 is equivalent to that of a photodiode, since both elements are performing conversion of light into electrical current. Thus it is inherent that the photoelectric conversion element 42 can be replaced with a photodiode of figure 3, column 2 line 62.

14. Applicant's arguments, see page 8, filed 3/27*2007, with respect to the rejection(s) of claim(s) 11 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Amano et al.

Conclusion

15. Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

16. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thi Le whose telephone number is (571) 270-1104. The Examiner can normally be reached on Monday-Friday from 7:30am to 5:00pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or 703-305-3028.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist/customer service whose telephone number is (571) 272-2600.

KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER

Thi Le